INTEGRATED CIRCUITS

DATA SHEET

74ABT162240
74ABTH162240

16-bit inverting buffer/driver with 30Ω series termination resistors

Product specification
Supersedes data of 1998 Jan 16
IC23 Data Handbook

1998 Feb 25

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16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

74ABT162240
74ABTH162240

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +12mA/-32mA
- TTL input and output switching levels
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH162240 incorporates bus hold data inputs which eliminate the need for external pull up resistors to hold unused inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT162240 is a high-performance BiCMOS device which combines low static and dynamic power dissipation with high speed.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables (1$\overline{\text{OE}}$, 2$\overline{\text{OE}}$, 3$\overline{\text{OE}}$, 4$\overline{\text{OE}}$), each controlling four of the 3-State outputs.

Two options are available, 74ABT162240 which does not have the bus hold feature and 74ABTH162240 which incorporates the bus hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25°C$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{\text{Y}}$x	C_L = 50pF; V_{CC} =	2.7 2.6	ns
C_{IN}	Input capacitance n$\overline{\text{OE}}$	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =	500	μA
I_{CCL}		Outputs low; V_{CC} = 5.5V	8	mA

ORDERING INFORMATION

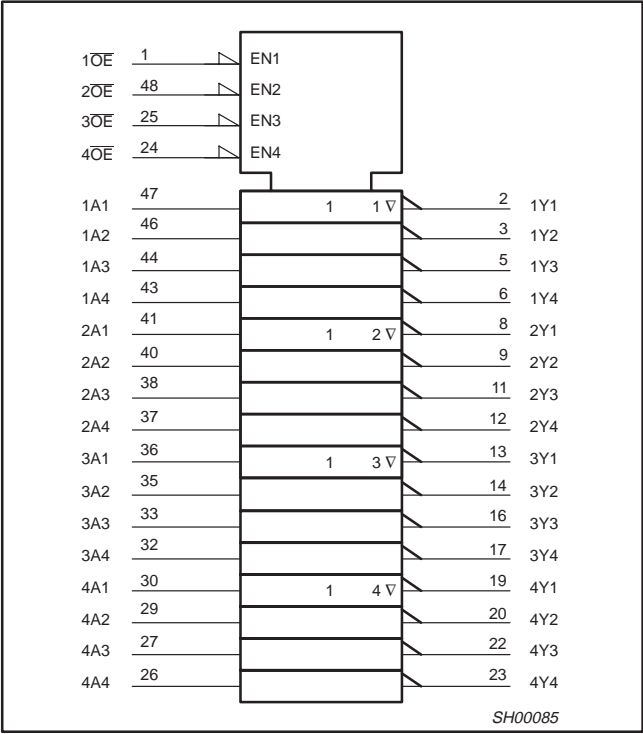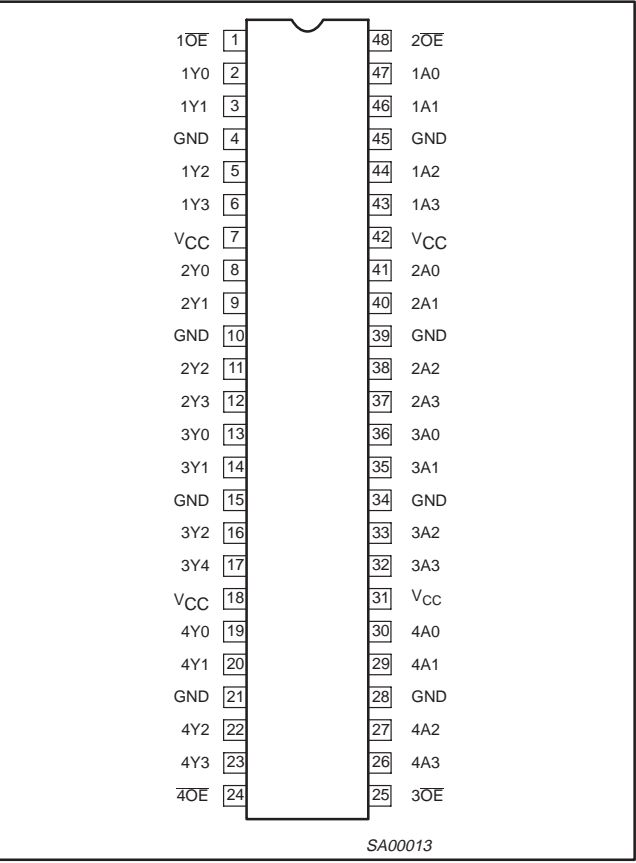| PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	−40°C to +85°C	74ABT162240 DL	BT162240 DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABT162240 DGG	BT162240 DGG	SOT362-1
48-Pin Plastic SSOP Type III	−40°C to +85°C	74ABTH162240 DL	BH162240 DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABTH162240 DGG	BH162240 DGG	SOT362-1

LOGIC SYMBOL
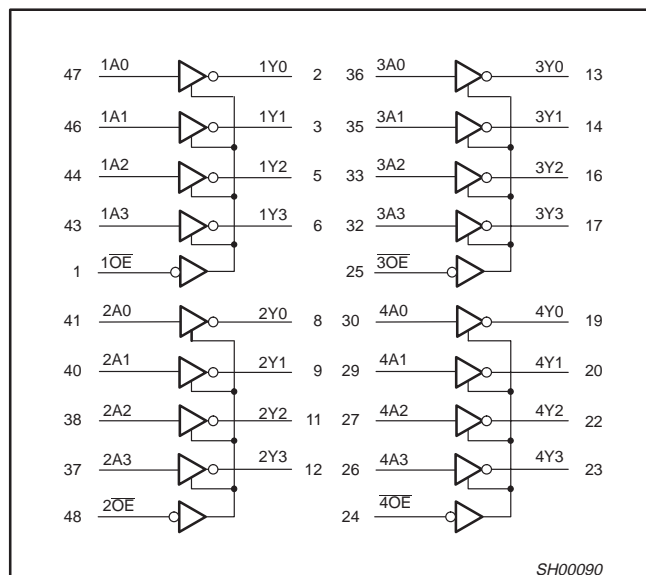
SH00090

16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

**74ABT162240
74ABTH162240**

LOGIC SYMBOL (IEEE/IEC)

Pin	Signal			Pin	Signal
1	1$\overline{\text{OE}}$		EN1		
48	2$\overline{\text{OE}}$		EN2		
25	3$\overline{\text{OE}}$		EN3		
24	4$\overline{\text{OE}}$		EN4		

1A1 47 — 1   1▽ — 2 1Y1
1A2 46 — 3 1Y2
1A3 44 — 5 1Y3
1A4 43 — 6 1Y4
2A1 41 — 1   2▽ — 8 2Y1
2A2 40 — 9 2Y2
2A3 38 — 11 2Y3
2A4 37 — 12 2Y4
3A1 36 — 1   3▽ — 13 3Y1
3A2 35 — 14 3Y2
3A3 33 — 16 3Y3
3A4 32 — 17 3Y4
4A1 30 — 1   4▽ — 19 4Y1
4A2 29 — 20 4Y2
4A3 27 — 22 4Y3
4A4 26 — 23 4Y4

SH00085

PIN CONFIGURATION

1$\overline{\text{OE}}$	1		48	2$\overline{\text{OE}}$
1Y0	2		47	1A0
1Y1	3		46	1A1
GND	4		45	GND
1Y2	5		44	1A2
1Y3	6		43	1A3
V$_{CC}$	7		42	V$_{CC}$
2Y0	8		41	2A0
2Y1	9		40	2A1
GND	10		39	GND
2Y2	11		38	2A2
2Y3	12		37	2A3
3Y0	13		36	3A0
3Y1	14		35	3A1
GND	15		34	GND
3Y2	16		33	3A2
3Y4	17		32	3A3
V$_{CC}$	18		31	V$_{CC}$
4Y0	19		30	4A0
4Y1	20		29	4A1
GND	21		28	GND
4Y2	22		27	4A2
4Y3	23		26	4A3
4$\overline{\text{OE}}$	24		25	3$\overline{\text{OE}}$

SA00013

FUNCTION TABLE

Inputs		Outputs
n$\overline{\text{OE}}$	nAx	n$\overline{\text{Y}}$x
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

SCHEMATIC OF Y OUTPUTS

SA00042
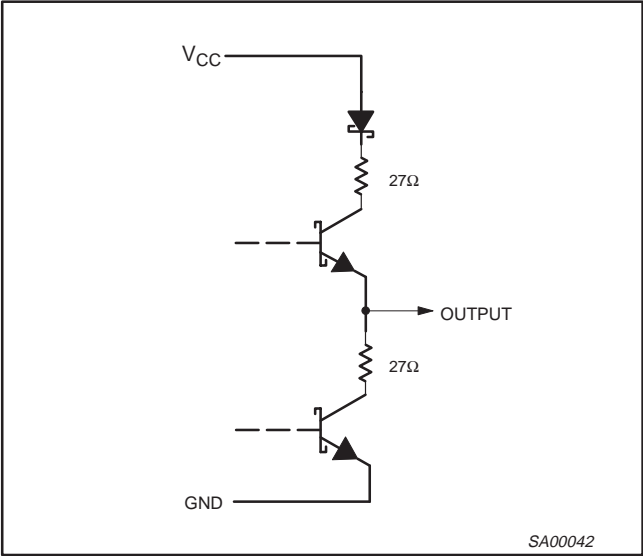
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	$1\overline{Y}0$-$1\overline{Y}3$ $2\overline{Y}0$-$2\overline{Y}3$ $3\overline{Y}0$-$3\overline{Y}3$ $4\overline{Y}0$-$4\overline{Y}3$	Data outputs
1, 48, 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		12	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

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16-bit inverting buffer/driver with 30Ω series
termination resistors (3-State)

74ABT162240
74ABTH162240

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} = +25°C Min	Typ	Max	T_{amb} = −40°C to +85°C Min	Max	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA			−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 8mA; V_I = V_{IL} or V_{IH}				0.65		0.65	V
		V_{CC} = 4.5V; I_{OL} = 12mA; V_I = V_{IL} or V_{IH}				0.80		0.80	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH162240	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0			−2	−3		−5	µA
I_{HOLD}	Bus Hold current A inputs[3] 74ABTH162240	V_{CC} = 4.5V; V_I = 0.8V		50			50		µA
		V_{CC} = 4.5V; V_I = 2.0V		−75			−75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±500					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = V_{CC}			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			−1.0	−10		−10	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−70	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1.0		1.0	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1.0		1.0	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT162240	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			10	200		200	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH162240	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			0.2	1.0		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This is the bus hold overdrive current required to force the input to the opposite logic state.

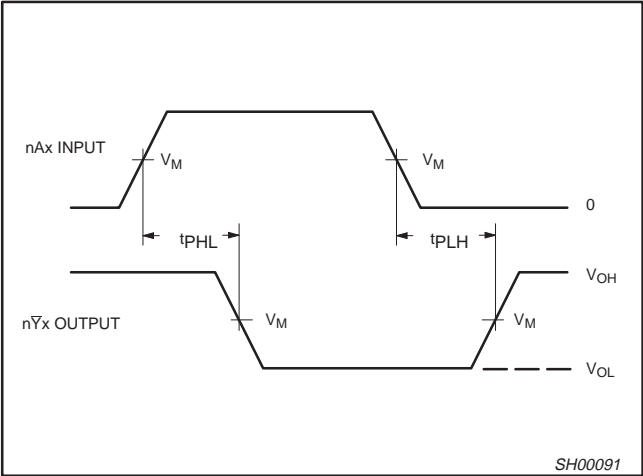## 16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = −40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	1.0 1.0	2.7 2.6	3.8 3.2	1.0 1.0	4.2 3.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.2 1.0	2.3 2.9	3.2 3.8	1.2 1.0	4.0 4.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.6 1.4	3.0 2.8	4.1 3.8	1.6 1.4	4.7 4.0	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

Waveform 1. Input (nAx) to Output (nYx) Propagation Delays
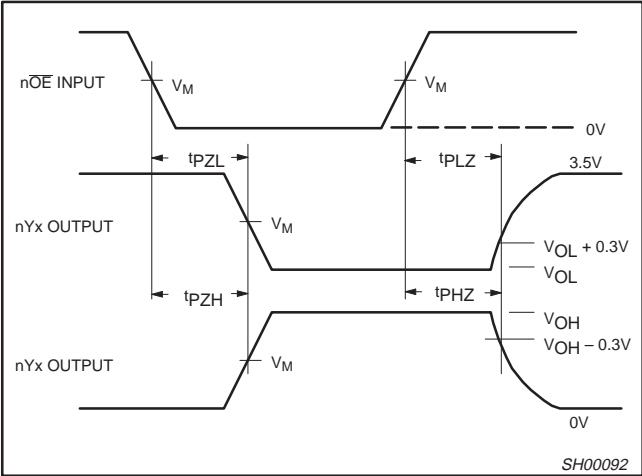
Waveform 2. 3-State Output Enable and Disable Times

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TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	7V
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

$V_M = 1.5V$
Input Pulse Definition

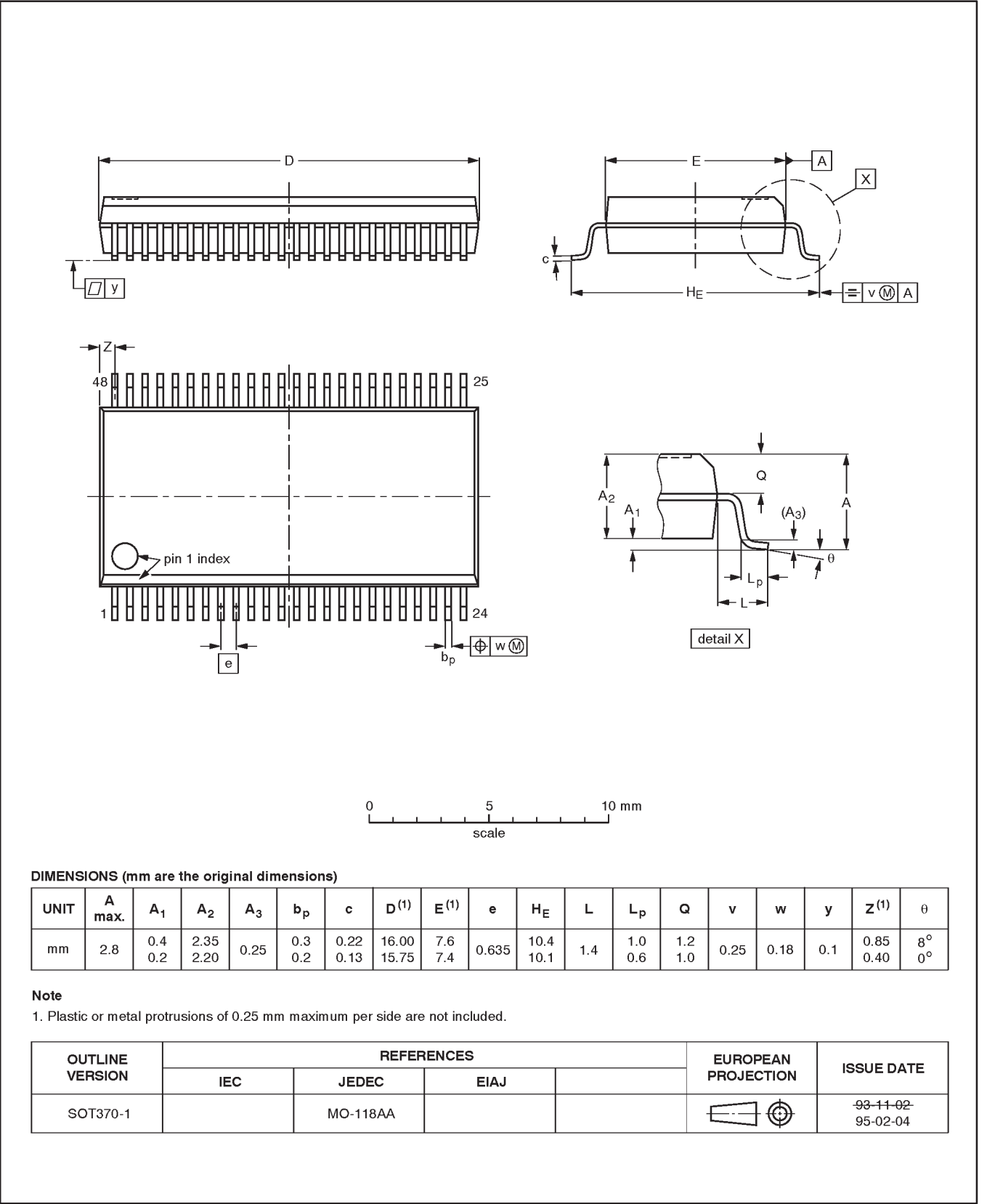| FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00093

16-bit inverting buffer/driver with 30Ω Series
Termination Resistors (3-State)

74ABT162240
74ABTH162240

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm   **SOT370-1**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[1]	e	H_E	L	Lₚ	Q	v	w	y	Z[1]	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm   **SOT362-1**

Dimensions in mm.

MSA399

detail X

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Product specification

16-bit inverting buffer/driver with 30Ω Series
Termination Resistors (3-State)

74ABT162240
74ABTH162240

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1]   Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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